1-13. (Cancelled)

14. (Currently Amended) ~~The method in accordance with claim 13 further comprising a step of:~~ A method for fabricating an interconnect system for providing a signal path to a first circuit node of an integrated circuit (IC) formed within and on a portion of a semiconductor wafer having horizontal upper and lower surfaces, the method comprising the steps of:

a. forming a hole extending vertically through an area of the semiconductor wafer adjacent to the portion of the wafer containing the IC,

b. placing the first conductive material in the hole, the first conductive material vertically extending through the hole,

c. conductively linking the first conductive material to the first circuit node, and

d. cutting the semiconductor wafer vertically along a horizontal ~~saw~~-line extending across the hole such that a portion of the semiconductor wafer containing the IC includes a peripheral edge formed along the saw-line upon which a portion of the first conductive material placed in the hole remains attached.

15. (Previously Presented) The method in accordance with claim 14 further comprising a step of:

e. forming a bond pad on the lower surface of the semiconductor wafer conductively linked to the conductive material placed in the hole.

16. (Previously Presented) The method in accordance with claim 14 further comprising a step of:

e. providing second conductive material extending horizontally from the first conductive material along and attached to the lower surface of the semiconductor wafer under the portion of the semiconductor wafer containing the IC.

17. (Previously Presented) The method in accordance with claim 14 wherein step c comprises a step of:

e. providing second conductive material extending horizontally on the upper surface of the semiconductor wafer and on the IC from the first conductive material to the first circuit node.

18. (Previously Presented) The method in accordance with claim 17 further comprising a step of:

f. providing third conductive material extending horizontally from the first conductive material along and attached to the lower surface of the semiconductor wafer under the portion of the semiconductor wafer containing the IC.

19. (Withdrawn) The method in accordance with claim 16 further comprising the steps of:

e. coating a portion of the conductive material extending along and attached to the lower surface of the portion of the semiconductor wafer containing the IC with resilient material, and

f. detaching the portion of the conductive material coated with resilient material from the lower surface of the portion of the semiconductor wafer containing the IC so that it forms a spring contact linked by the conductive material to the first circuit node.

20-36. (Cancelled).

37. (Currently Amended) ~~The method in accordance with claim 36 further comprising the step of:~~ The method for fabricating an interconnect system of claim 14 further providing for additional signal paths between additional circuit nodes formed within and on the semiconductor wafer, the method comprising the steps of:

a. forming additional holes extending vertically through the semiconductor wafer in areas of the semiconductor wafer between areas defining IC dice,

b. placing additional first conductive material in the additional holes formed in the semiconductor wafer,

c. placing second conductive material on the upper surfaces of wafer forming an upper surface of the IC dice, the second conductive material forming signal paths extending horizontally between the additional circuit nodes and the first conductive material placed in the holes, and

d. cutting the wafer in the areas between the dice along a line extending through the additional holes so as to singulate the IC dice and so that portions of the first conductive material remain on the IC dice after the IC dice are singulated to provide conductive paths between the second conductive material on the upper surfaces of the IC dice and lower surfaces of the IC dice.

38. (Previously Presented) The method in accordance with claim 37 further comprising the step of:

e. prior to cutting the wafer at step d, forming conductive pads on the lower surfaces of the IC dice that are conductively linked to the first conductive material placed in the holes.

39. (New) The method in accordance with claim 14 further comprising the step of:

e. prior to cutting the wafer at step d, forming conductive pads on the lower surfaces of the IC dice that are conductively linked to the first conductive material placed in the holes.